REMARKS

1. Claims 1-46 and 50-54 were pending. Claims 11, 15, 21-23, 39, 45, and 53 have been cancelled. Claims 5, 13, 18, 19, 27, 29, 31, 37, 43, 44, 50, 51, and 54 have been amended. Claims 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, and 54 are now pending. Reexamination and reconsideration of the application, as amended, are requested.

2. Rejections under 35 U.S.C. § 112 ¶ 2

On page 2 of the Office Action, Claims 11, 13-17, 19-21, 27, 29-36, 43-46, and 51-53 were rejected under 35 U.S.C. § 112 ¶ 2. Of these claims, Claims 11, 15, 45 and 53 have been cancelled and the other claims have been amended to more particularly point out and distinctly claim that which the Applicants regard as their invention. Withdrawal of the rejection is requested.

3. Rejection under 35 U.S.C. § 103(a)

Claims 13-16 were rejected in the Office Action under 35 U.S.C. § 103(a) as being unpatentable over Kasai (US Patent No. 5,821,594). Claims 13-14 and 17 were rejected in the Office Action under 35 U.S.C. § 103(a) as being unpatentable over Mele et al. (US Patent No. 5,037,777). Claims 18-22, 24-29, 37-38, 40-44, 46, 50-52, and 54 were rejected in the Office Action under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. (US Patent No. 5,677,227). The Applicants respectfully traverse the rejections and request consideration of the following.

4. The Office Action allowed Claims 1-10 and 12, and also indicated that Claims 11, 23, 30, 31-36, 39, 45, and 53 would be allowable if rewritten. Accordingly, the relevant limitations of Claim 23 have been added into Claim 18, the relevant limitations of Claim 39 have been added into Claim 37, the relevant limitations of Claim 45 have been added into Clam 44, and the relevant limitations of Claim 53 have been added into Claim 50. As such, Claims 1-10, 12, 18-20, 24-38, 40-44, 46, 50-52, and 54, as amended, are allowable.

5. The Office Action indicated Claim 1 to be allowed. Claim 1 recites that an etch of doped silicon dioxide has a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide layer or for a semiconductor. A like limitation has added to Claim 13. As such, amended independent Claim 13 is allowable, as are Claims 14, 16, and 17 that depend therefrom.

6. In sum, the Applicant respectfully submits that, as to the claims now pending, a *prima facie* case of obvious has not been made out, or in the alternative, the pending claims avoid the rejection. As such, the Applicant respectfully maintains that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of Claims 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, and 54 at an early date is solicited.

7. **Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):**

Amend Claims 5, 13, 18, 19, 27, 29, 31, 37, 43, 44, 50, 51, and 54 as follows and in accordance with 37 C.F.R. § 1.121(c)(1)(ii), by which the Applicants submit the following marked up version only for claims being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

5. (Once Amended) A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3

13. (Twice Amended) A process for forming contact to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of monocrystalline silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist;

etching said doped silicon dioxide layer through the pattern of said layer of photoresist at a material removal rate that is higher for doped silicon dioxide layer than for undoped silicon dioxide layer or for said layer of monocrystalline silicon to form an opening extending to said layer of monocrystalline silicon, said etching being [in] a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3

with a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, and CH_3F.

18. (Twice Amended) A process for forming a contact to a semiconductor substrate comprising:

providing a gate oxide layer over the semiconductor substrate;

providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and an undoped silicon dioxide layer extending over said conductive layer;

forming a spacer, composed of undoped silicon dioxide, adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer[material], and the semiconductor substrate.

19. (Once Amended) A process as recited in Claim 18, wherein each said gate stack is formed by[further comprising]:

forming polysilicon layer over said gate oxide layer;

forming a refractory metal silicide layer over said polysilicon layer; and

forming an undoped silicon dioxide layer over said refractory metal silicide layer.

27. (Once Amended) A process as recited in Claim 20[21], wherein said refractory metal silicide layer is tungsten silicide.

29. (Once Amended) A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist; and

etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3; and

with a fluorinated chemical etchant.

31. (Twice Amended) A process for forming a contact to a semiconductor material comprising:

depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

depositing a polysilicon layer over said gate oxide layer;

depositing a refractory metal silicide layer over said polysilicon layer;

depositing an undoped silicon dioxide layer over said refractory metal silicide layer;

selectively removing portions of said undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side perpendicular to said gate oxide layer and being comprised of:

said undoped silicon dioxide layer as the top layer thereof;

said refractory metal silicide layer;

said polysilicon layer; and

said gate oxide layer as the bottom layer thereof;

forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

etching said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 in an etcher selected from the group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, and CH_3F.

37. (Twice Amended) A process for forming a gate structure comprising:

providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

removing said first layer of photoresist;

depositing a doped silicon dioxide layer over said multilayer structure;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch that is an anisotropic plasma etch using fluorinated chemical etchants selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, and CH_3F, and that etches through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material;

removing said second layer of photoresist; and

forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

43. (Twice Amended) A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch is a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 ions/cm^3[3] to about 10^{13} ions/cm^3[3]; and

with a fluorinated chemical etchant.

44. (Twice Amended) A process for forming a gate structure comprising:

providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

removing said first layer of photoresist;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG;

forming a second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical

etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, and CH_3F, wherein said etching of said doped silicon dioxide utilizes a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

removing said second layer of photoresist; and

forming a contact plug comprising a conductive material in contact with said contact surface on said layer of silicon.

50. (Twice Amended) A method of forming a self-aligned contact, said method comprising:

providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by an undoped silicon dioxide layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

forming a layer of photoresist over said silicon dioxide layer;

patterning said layer of photoresist; and

selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks using an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, and CH_3F to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing less of said undoped silicon dioxide

layer over said pair of gate stacks than doped silicon photoresist, said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

51. (Once Amended) A method as recited in Claim 50, wherein said selective removal of said doped silicon dioxide layer comprises [etching said doped silicon dioxide layer in] a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C; and

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3[; and

with a fluorinated chemical etchants].

54. (Once Amended) A method as recited in Claim 51[0], wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for semiconductor material.

8. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 30 day of November, 2000.

Respectfully submitted,

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